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HIGH SPEED WIDE FAN-IN DATA SELECTOR USING CURRENT COMPARISON DOMINO IN SYNOPSYS HSPICE

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ABSTRACT

In this paper, we tend to implement seven circuit topologies of domino to boost the speed and to lower the consumption of total power. Domino logic circuits are used for prime performance and high speed applications. A data selector circuit is proposed based on new high speed and noise immune domino logic circuit named as Current Comparison based Domino (CCD). The CCD reduces parasitic capacitance implies to small keeper and low leakage current, which results fast, robust and improved noise immune design for wide fan-in (64-input) gates. The logic circuits are simulated using Synopsys HSPICE tool with 16-nm V2.1 high-performance predictive technology models at 110 °C and 0.8 V supply voltage. The simulation results unconcealed that prime speed of CCD offers the most effective in terms of noise-immunity and power consumption at the constant delay are compared with standard domino circuit for 64-bit OR gates. The data selector (Mux) logic is implemented in CCD logic.

KEYWORDS: Domino logic, CCD, keeper ratio, leakage current, PDN, PUN, wide fan-in, data selector.

INTRODUCTION

The tentative rise in contemporary technology scenario, now-a-days needs low-power, high-speed VLSI systems with strengthen performance. One of the most widely used logics in VLSI architecture are domino logic. Domino logic circuits are widely used for tremendous performance in critical units such as microprocessors and high speed implementation of wide fan- in circuits. Domino logic is the best approach which overcomes the drawback of dynamic logic. The main drawback of dynamic logic is that cascading of two different dynamic logics stages failed and it declines the Monotonicity principle. To overcome that, we go for domino logic. The drawback of dynamic logic is eliminated by simply inserting a static inverter between two stages. This resembles two dynamic logics are connected using a static logic inverter. As the technology shrinks the threshold voltage (V*th*) of the transistor also lowers in the same proportionate. Scaling of threshold voltage outcomes in exponential increase of sub threshold leakage current in the evaluation transistor and causes the domino logic little noise immune due to more parallel leaky paths of wide fan-in gates. The main source of noise in deep-submicron circuit is mainly due to more leakage current, crosstalk, input noise and charge sharing, while noise at the input of the evaluation transistor enhances noise because of increased crosstalk. In domino logic reducing the supply voltage and capacitance of dynamic node (pre-charge) decreases the total charge stored at the dynamic node. Because of all these concurrent factors, the noise immunity of domino gate substantially reduces with technology scaling. The leakage current is more problematic in high fan-in domino circuits because of larger leakage due to more parallel evaluation paths.

An enhanced domino logic is proposed which has low leakage without dramatic speed degradation for wide fan-in gates. This technique uses the concept of current comparison based domino (CCD) logic.

This paper is organized as follows: section II revises the literature review. Section III discusses various advanced wide fan-in domino circuits followed by proposed technique in section IV. Coming to V explains the results and section VI discusses the designing of data selector (Mux) using CCD. Finally section VII concludes the paper.

LITERATURE REVIEW

The more often used dynamic logic is the traditional standard footless domino circuit (SFLD). In this diagram, a pMOS keeper transistor is used to avoid the unnecessary discharging at the dynamic node as a result of leakage currents and charge sharing of the pull-down network (PDN) at the time of evaluation phase, so that improving the robustness. The keeper ratio *K* is defined as shown in equation (1)

$$K = \frac{\mu p\ (W/L)\text{Keeper}-\text{transistor}}{\mu n\ (W/L)\text{evaluation}-\text{network}} \quad \ldots\ldots\ldots\ldots \quad (1)$$

where *W* and *L* denotes the width and length of transistor size, and μ_p and μ_n are the hole and electron mobilities, respectively. However, the conventional keeper approach has fewer effective in new generations of CMOS technology. Although keeper upsizing improves noise immunity, it increments the contention current in between the keeper transistor and the evaluation network.

Thus, it increments power consumption and evaluation delay of standard footless domino circuits. These problems are more critical in wide fan-in dynamic gates because of more number of leaky nMOS transistors connected to the dynamic node as shown in fig (1) Standard Footless Domino (SFLD).

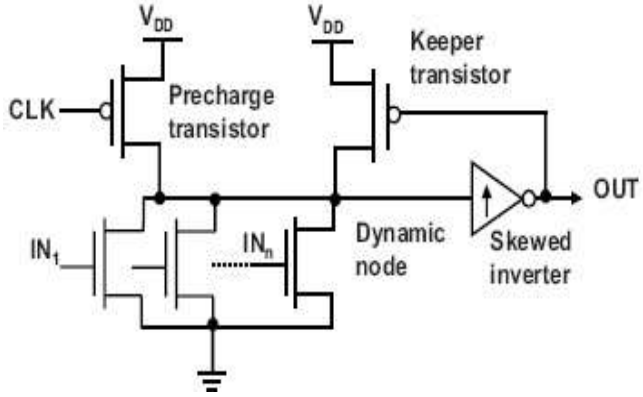

Fig. 1. Standard Footless Domino

EXHISTED TECHNOLOGIES

Several circuit techniques are proposed here. These circuit techniques can be divided into two categories. In the first category, circuit techniques that changes the controlling circuit of the gate voltage of the keeper such as conditional-keeper domino (CKD), high-speed domino (HSD), leakage current replica (LCR) keeper domino, and controlled keeper by current-comparison domino (CKCCD) respectively. On the other hand, in the second category, designs including the proposed designs change the circuit topography of the footer transistor or reengineer the evaluation network such as diode-footed domino (DFD) and diode-partitioned domino (DPD).

Conditional Keeper Domino(CKD) :

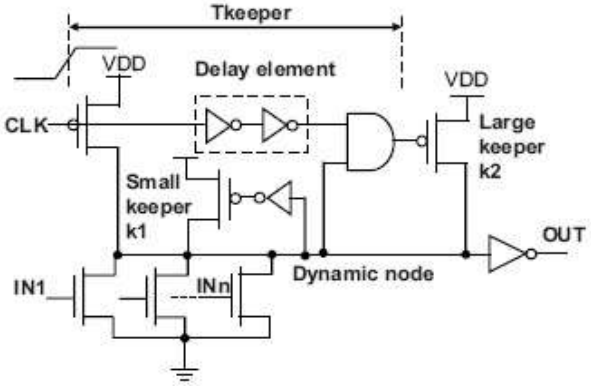

Fig. 2. Conditional Keeper Domino

This consists of small and large keeper transistors. The conditional keeper domino has some disadvantages such as limitations on increasing the delay and power dissipation due to upsizing as shown in fig (2), Conditional Keeper Domino (CKD).

High Speed Domino (HSD) :

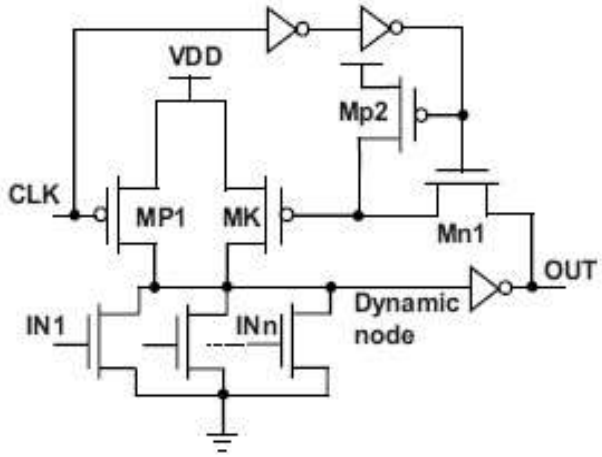

Fig. 3. High Speed Domino

Reduce the current drawn through the PMOS keeper and the nMOS Pull Down Network. This is in keeping the large pMOS keeper without performance degradation and leakage current. However the power and area overhead of the clock delay circuit will exhibits as shown in fig (3), High Sped Domino (HSD).

Leakage Current Replica Keeper (LCR Keeper) :

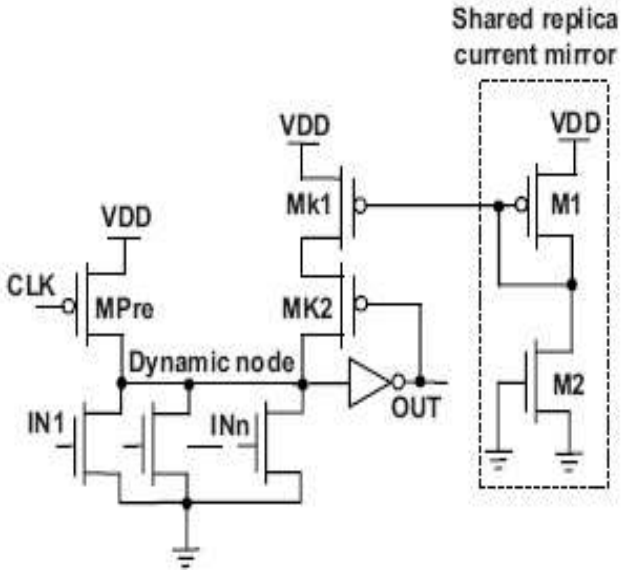

Fig. 4. Leakage Current Replica Keeper

It improves scaling of the dynamic logic gates, but area is increased as shown in fig (4), Leakage Current Replica (LCR).

Controlled Keeper by Current-Comparison Domino (CKCCD) :

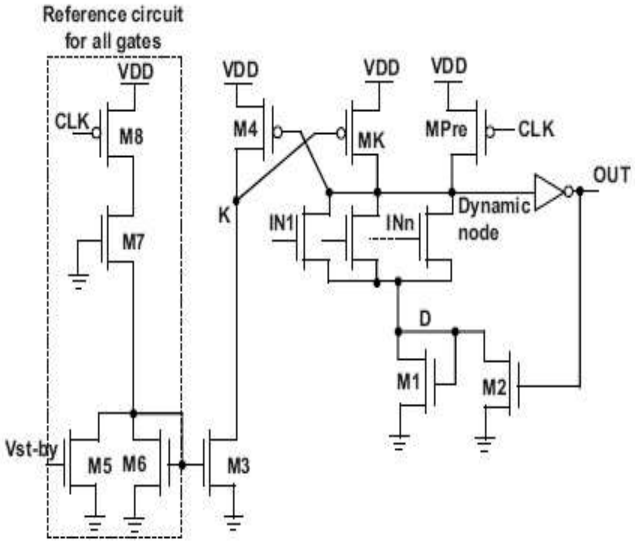

Fig. 5. Controlled Keeper Current Comparison Domino

It works on devaluation of leakage current and power but yet it suffers from major efficiency issues in terms of area and delay as shown in Controlled Keeper Current Comparison Domino (CKCCD).

Diode-Footed Domino (DFD):

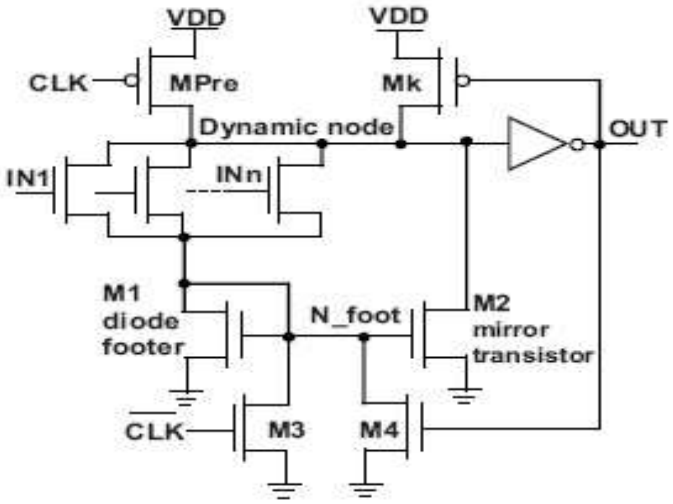

Fig. 6. Diode Footed Domino

A diode footer transistor is used in series with the evaluation network. So noise and robustness of this circuit increases more. For equal noise margin, more legs are possible. Gate is faster with equal number of gates. A fairly large safety factor is needed to account for the random on- die process variation especially FET Vt variation as shown in fig (6) Diode Footed Domino.

The drawbacks figured out with the existing works are increase in leakage current, noise immunity, area decrease in contention current robustness, power consumption, delay speed etc., especially for wide fan-in gates.

CURRENT COMPARISON BASED DOMINO (CCD) :

Consider the wide fan-in gates, the speed is dramatically decreased since the capacitance on the dynamic node is huge. Even though, increasing the size of keeper transistor can improve power consumption, delay and noise robustness are

increased due to large contention. Since upsizing of transistor *M*2 increases the speed, the mirror ratio *M* as shown in equation is defined as the ratio of the size of transistor *M*2 to the size of transistor *M*1

$$M= \frac{(W/L)M2}{(W/L)M1} \quad \text{……..…..} \quad (2)$$

With reference to the circuit schematic shown in Fig. 2a, two phases of the proposed circuit are explained in detail as follows.

These problems could be solved if the PDN implements logical function, is separated from keeper transistor by using a comparison stage in which the worst case leakage current. This idea is illustrated in Fig. 7.a. Where PUN is used instead of PDN.

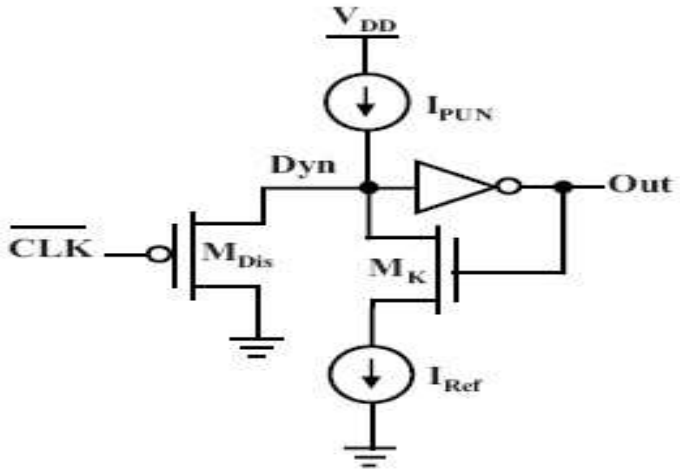

Fig. 7 .a. Concept of CCD

Transistor MK is added in series with the reference current I_{Ref} to decrease the total power consumption when the voltage of the node at the output has fallen to ground voltage. Another important issue in the generation of reference current according to the process variation in order to maintain the robustness of the proposed circuit.

In the proposed CCD circuit, the effects of any threshold voltage variations on the voltage of nodes A and B is important because it directly affects the speed of the gate, noise immunity and consequently power consumption.

An important concern in the generation of the reference voltage, which is the correct variation of the reference current I_{Ref} conferring to the process variations to maintain the robustness of the proposed circuit. Process variations are due to systematic and random parameter fluctuations. Here systematic variations are considered. We have assumed that in a given circuit design the threshold voltage of all nMOS transistors varies together and that of pMOS transistors varies together. The worst scenario is that the threshold voltage of nMOS transistors is decreased and that of the pMOS transistors is increased, i.e., slow pMOS and fast nMOS due to process variations. In the former case, the subthreshold leakage of pMOS transistors of the Pull Up Network is decreased, thus the reference current must be reduced and vice versa for the next case. Hence, the reference current must be varied according to threshold voltage variations to maintain robustness in the design. To track process variations in dynamic logic circuits, several solutions are proposed in the literature by using a process variation sensor, such as one based on drain-induced barrier lowering (DIBL) effect, rate sensing keeper, and replica keeper current [6]. In the proposed circuit, a replica circuit like that proposed by [6] can be used as a leakage current sensor for proper operation and superior performance, in the worst case of fan-in, which is a 64-input OR gate because of it has very high leakage current among other gates.

The proposed circuit used for generating the reference current for all gates is shown in Fig. 7(b). It is similar to the replica leakage circuit proposed by [7], in which a series diode-connected transistor M_6 similar to M_1 is added. This circuit was the replica of the worst case leakage current $I_{Leakage\text{-}current}$ of the Pull Up Network to correctly track leakage current variations as a result of process variations. Therefore, the transistor M_7 gate is connected to V_{DD}, and its size

is derived from the sizes of pMOS transistors of the PUN in the worst case, which is a 64-input OR gate, and hence its width is set equal to the sum of the widths of 64 pMOS transistors of the PUN.

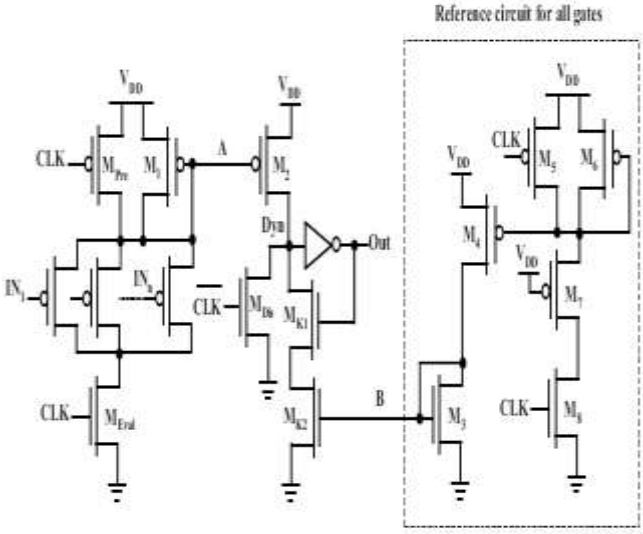

Fig. 7.b. Implementation of a wide fan-in OR gate

Predischarge Phase:

Clock and Input signals and voltage are in low and high levels, respectively, [CLK = "0", CLK = "1" in Fig. 7b in this phase. Therefore, the voltages of the dynamic node (Dyn) and node A have fallen to the low level by transistor M_{Dis} and rose to the high level by transistor Mpre, respectively. Hence, transistors M_{pre}, M_{Dis}, M_{k1}, and M_{k2} are on and transistors M_1, M_2, and M_{Eval} are off. Also, the output voltage is raised to the high level by the output inverter.

Evaluation Phase

In this phase, clock voltage is in the high level [CLK = "1", CLK = "0" in Fig. 2(b)] and input signals can be in the low level. Hence, transistors M_{pre} and M_{Dis} are off, transistorM_1, M_2, M_{k2}, and M_{Eval} are on, and transistor M_{k1} can be come on or off depending on input voltages. Thus, two states may occur. First, all of the input signals remain high. Second, at least one input falls to the low level. In the first state, a small amount of voltage is established across transistor M_1 due to the leakage current. Although this leakage current is mirrored by transistor M_2, the keeper transistors of the second stage (M_{k1} and M_{k2}) compensate this mirrored leakage current. It is clear that upsizing the transistor M_1 and increasing the mirror ratio (M) increase the speed due to higher mirrored current at the expense of noise-immunity degradation.

The waveforms are obtained by HSPICE simulator in the 16-nm high-performance V2.1 predictive technology models (PTMs) [1] at 110°C and 0.8 V supply voltage. In this simulation, only one input of an OR gate with 32 inputs falls to the low level in the evaluation phase. The simulation is performed by setting *Wp/Wn* = 2 for the output inverter, CL = 5 fF, and minimum size for the other transistors.

RESULTS

Results are drawn between Unity Noise Gain (UNG), Average Power (P_{Avg}), Power Delay Product (PDP), Energy Delay Product (EDP) verses number of inputs are drawn at a constant delay. The delays for 8_input, 16_input, 32_input, 64_input are 50ps, 50ps, 60ps, 70ps respectively.

The Unity Noise Gain (UNG), is equal to the amplitude of the input noise that results the same amplitude to appear at the output. It explains in equation (2) and the units are p_sec

$UNG = \{V_{in} : V_{Noise} = V_{output}\}$ .....(2)

Input	SFLD	CKD	HSD	LCR Keeper	CKCCD	DFD	CCD

8	0.9992	0.9953	0.9968	0.9997	1.0002	0.9992	1.0003
16	0.9993	0.9955	0.9974	0.9976	1.001	0.999	1.002
32	0.9972	0.9929	0.9945	0.9982	1.0003	0.9972	1.004
64	0.9937	0.9981	0.9902	0.9927	1.0005	0.9932	1.005

TABLE I. UNITY NOISE GAIN VERSES NO. OF INPUTS AT THE CONSTANT DELAY

Input	SFLD	CKD	HSD	LCR Keeper	CKCCD	DFD	CCD
8	0.2577	0.2403	0.2471	0.1803	0.164	0.1346	0.1058
16	0.2793	0.2565	0.2687	0.2417	0.1769	0.1807	0.1196
32	0.3477	0.2827	0.3097	0.1282	0.2207	0.17	0.1326
64	0.4087	0.3205	0.3631	0.3154	0.2696	0.219	0.1838

TABLE II. AVERAGE POWER VERSES NO. OF INPUTS AT THE CONSTANT DELAY

Input	SFLD	CKD	HSD	LCR Keeper	CKCCD	DFD	CCD
8	1.29E-15	1.21E-15	1.24E-15	9.12E-16	8.28E-16	6.75E-16	5.33E-16
16	1.40E-15	1.30E-15	1.35E-15	1.21E-15	8.86E-16	9.09E-16	5.55E-16
32	2.08E-15	1.70E-15	1.88E-15	7.72E-16	1.33E-15	1.03E-15	7.97E-16
64	2.87E-15	2.26E-15	2.55E-15	2.21E-15	1.90E-15	1.54E-15	1.29E-15

TABLE III. POWER DELAY PRODUCT VERSES NO. OF INPUTS AT THE CONSTANT DELAY

Input	SFLD	CKD	HSD	LCR Keeper	CKCCD	DFD	CCD
8	6.49E-26	6.13E-26	6.25E-26	4.62E-26	4.18E-26	3.38E-26	2.69E-26
16	6.98E-26	6.62E-26	6.73E-26	6.07E-26	4.43E-26	4.57E-26	2.82E-26
32	1.25E-25	1.02E-25	1.14E-25	4.85E-26	8.05E-26	6.28E-26	4.79E-26
64	2.02E-25	1.59E-25	1.80E-25	1.55E-25	1.36E-25	1.09E-25	9.10E-26

TABLE IV. ENERGY DELAY PRODUCT VERSES NO. OF INPUTS AT THE CONSTANT DELAY

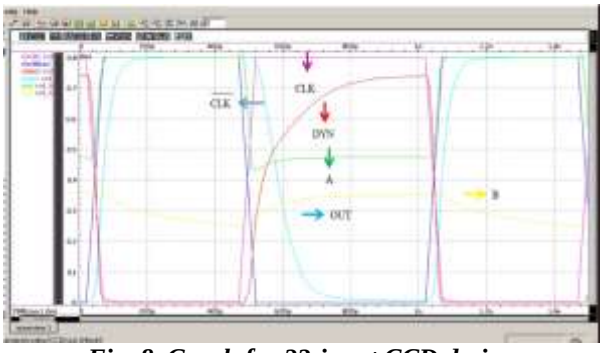

Fig. 8. Graph for 32-input CCD design

The graphs are drawn for UNG, Average Power P_{Avg}, PDP, EDP are drawn at a constant delays say 50ps, 50ps, 60ps, 70ps for 8_input, 16_input, 32_input, 64_input respectively.

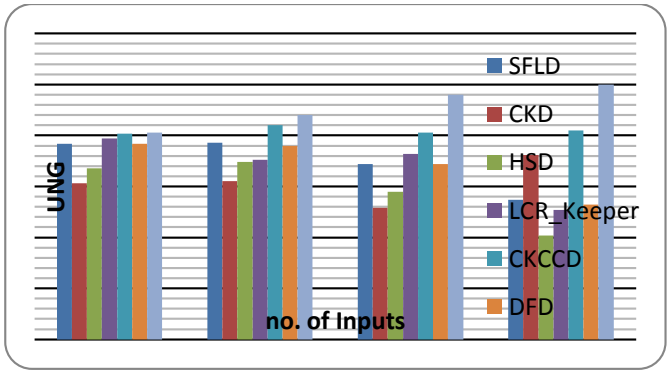

Fig. 9. Graph between UNG verses number of input at constant delay

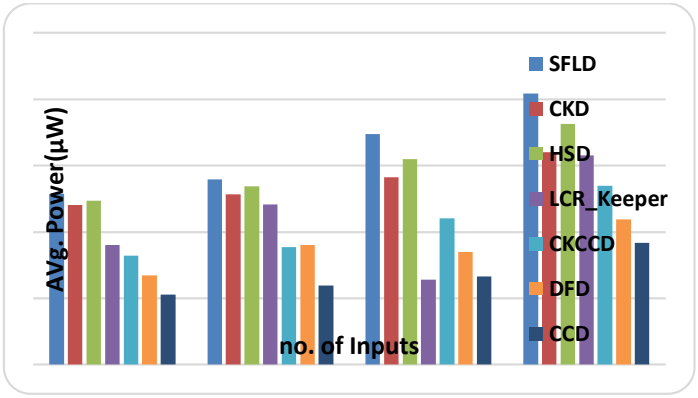

Fig. 10. Graph between Average Power verses number of input at constant delay

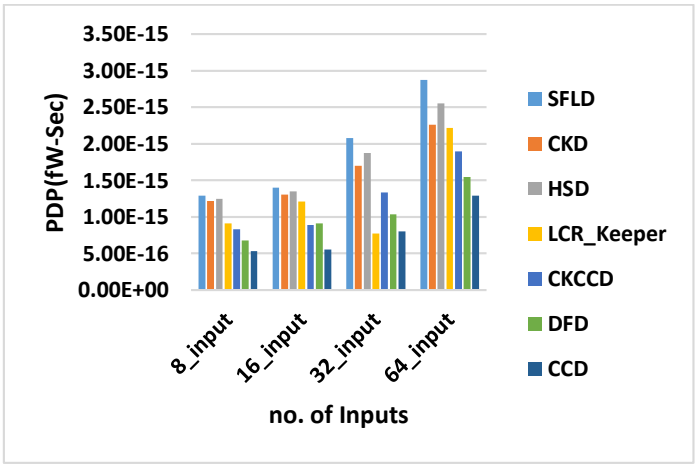

Fig. 11. Graph between Power Delay Product verses number of input at constant delay

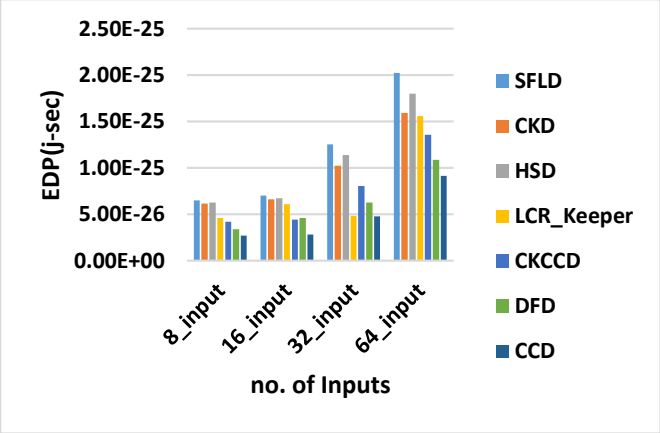

Fig. 12. Graph between Energy Delay Product verses number of input at constant delay

DESIGNING OF DATA SELECTOR USING CCD

The data selector or Mux is of size 64:1. The mux input is 64 i.e, it has 6 selection lines and 64 input lines as shown in figure 13. This logic is implemented in current comparison based domino using PUN. The logic of OR gate is replaced with 64 input data selector.

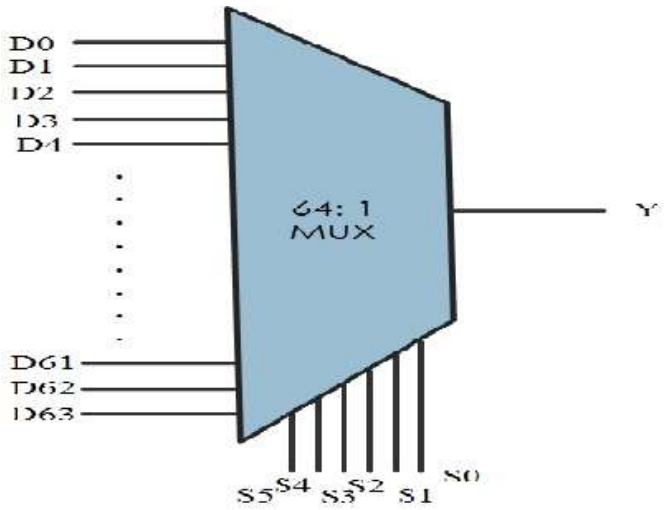

Fig. 13. 64:1 Mux or Data Selector

The proposed multiplexer is compared with the existing Diode Footed Domino multiplexer. Mostly multiplexers are used in register files of the processor memory as data selectors. So it is very important that power dissipation for the multiplexers should be very less. The proposed data selector shown in the figure is a 64:1 multiplexer. S0 to S5 are the select lines and D0 to D63 are the data input lines. From the results it is seen that the proposed data selector has low power dissipation, improved noise, better delay on comparison with all other multiplexer designs.

CONCLUSION

The leakage current of the evaluation network of dynamic gates was dramatically increased with technology scaling, especially for wide domino gates, yield got reduced noise immunity and increased power consumption. Thus, new designs were required to obtain required noise robustness in very wide fan-in circuits. Moreover, increasing the fan-in not only improves the worst case delay, but also increased the contention between the keeper transistor and the evaluation network. The best circuit design that we called CCD was proposed in this paper and followed by a multiplexer of 64:1 has robust design and very high performance. The main goal was to make the domino circuits more robust and with very low leakage and without significant speed degradation or increased power consumption with better performance. This can be observed by comparing the evaluation current of the gate with the leakage current.

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REFERENCES

[1] A.Peravi and M.Asyaei, "Current-Comparison-Based Domino: New Low-Leakage High-Speed Domino Circuit for Wide Fan-In Gates", VLSI SYSTEMS., Vol.45, no.1, pp.934-943-2013.
[2] Predictive Technology Model (PTM). 16 nm High Performance V2.1 Technology of PTM Model. (2012, Feb.19)[Online].Available:http://www.eas.asu.edu/ptm/
[3] H. Mahmoodi and K. Roy, "Diode-footed domino: A leakage-tolerant high fan-in dynamic circuit design style," IEEE Trans. Circuits SysI, Reg. Papers, vol. 51, no. 3, pp. 495–503, Mar. 2004.keeper for dynamic circuits," IEEE J. Solid-State Circuits, vol. 42, no. 1.
[4] A. Alvandpour, R. Krishnamurthy, K. Sourrty, and S. Y. Borkar, "A sub-130-nm conditional-keeper technique," IEEE J. Solid-State Circuits, vol. 37, no. 5, pp. 633–638, May 2002.
[5] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," IEEE Trans. Very Large Scale (VLSI) Syst., vol. 10, no. 2,pp. 71–78, Apr. 2002.
[6] Y. Lih, N. Tzartzanis, and W. W. Walker, "A leakage current replica keeper for dynamic circuits," IEEE J. Solid-State Circuits, vol. 42, no. 1, pp. 48–55, Jan. 2007.
[7] A. Peiravi and M. Asyaei, "Robust low leakage controlled keeper by current-comparison domino for wide fan-in gates, integration," VLSI J., vol. 45, no. 1, pp. 22–32, 2012.
[8] H. Suzuki, C. H. Kim, and K. Roy, "Fast tag comparator using diode partitioned domino for 64-bit microprocessors," IEEE Trans. Circuits Syst., vol. 54, no. 2, pp. 322–328, Feb. 2007.
[9] N. Shanbhag, K. Soumyanath, and S. Martin, "Reliable low-power design in the presence of deep submicron noise," in Proc. ISLPED, 2000, pp. 295–302.
[10] K. Roy, S. Mukhopadhyay, and H. Mahmoodi- Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.